

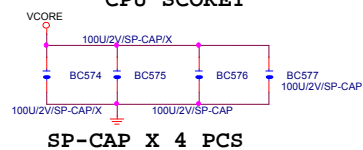
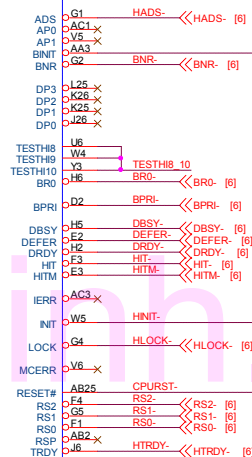
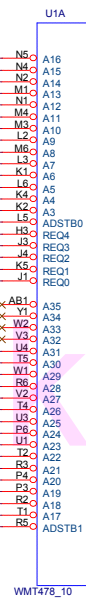
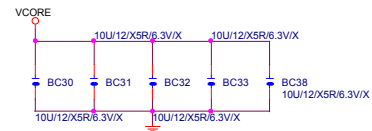
GIGABYTE GA-8IE2004P
Schematics

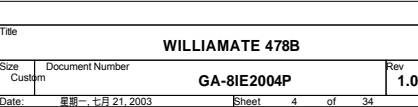
Revision 1.0

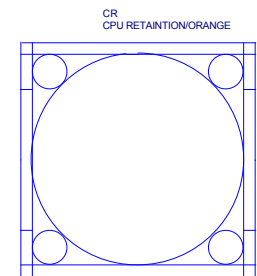
SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	WILLIAMATE_478A
04	WILLIAMATE_478B
05	WILLIAMATE_478C
06	MCH-BROOKDALE-E_A
07	MCH-BROOKDALE-E_B
08	MCH-BROOKDALE-E_C
09	MD0~63
10	DDR1~2
11	DDR-TERM
12	AGP
13	ICH4_1
14	ICH4_2
15	FWH (SINGLE BIOS)
16	ICS950223 CLOCK GEN
17	PCI1_2
18	PCI3_4
19	PCI5
20	ITE LPC I/O
21	IDE
22	KB_PS2

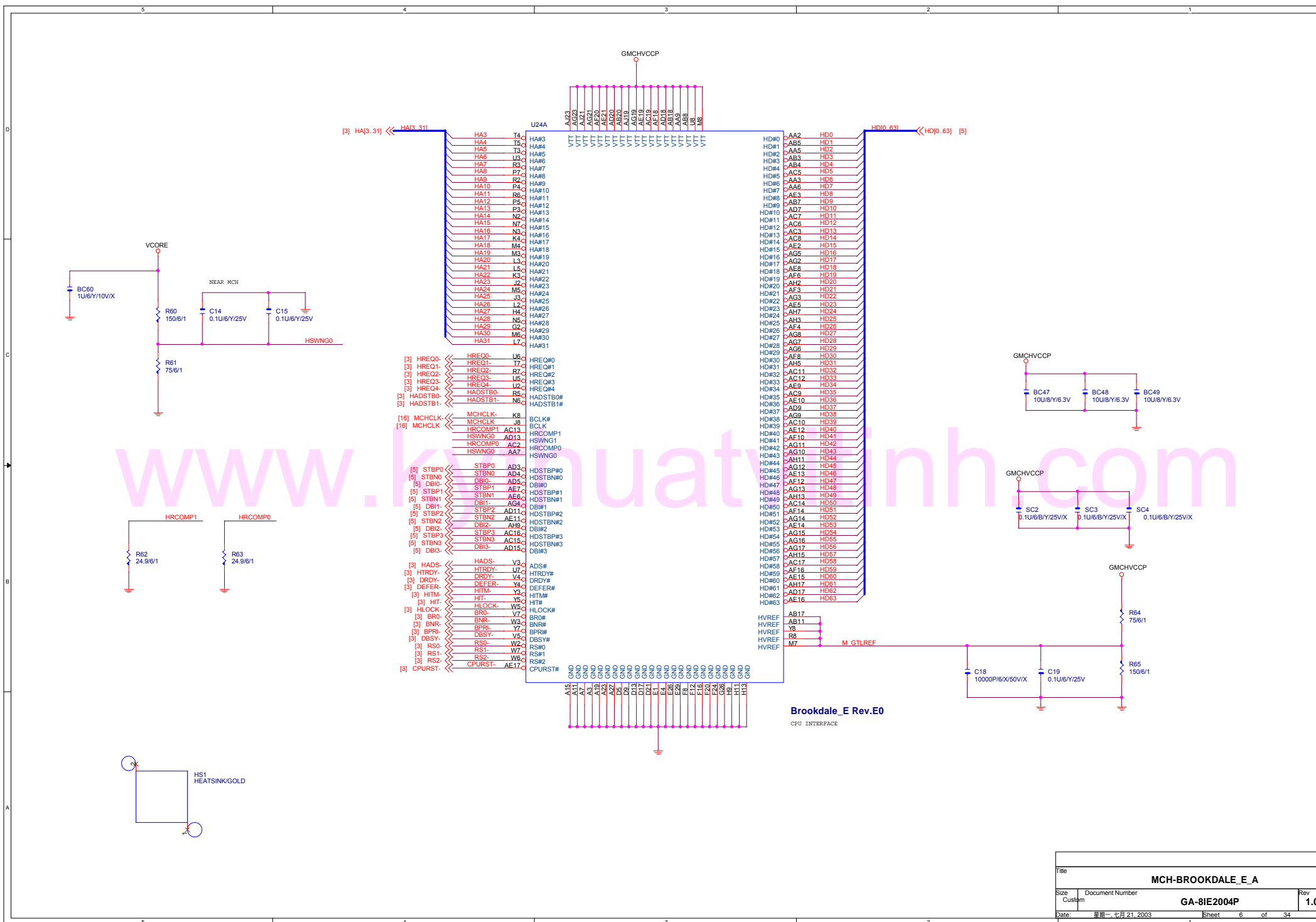
SHEET	TITLE
23	COM_LPT_FDD
24	F-USB1 & F-USB2
25	FPANEL
26	CODEC
27	AUDIO_GAMEPORT
28	AUDIO_SPDIF
29	DDR POWER
30	POWER1
31	POWER2
32	LAN RTL8100C & B-USB CONNECTOR
33	GPIO LIST
34	PCI ROUNT LIST
35	
36	
37	
38	
PCB	4v藍C

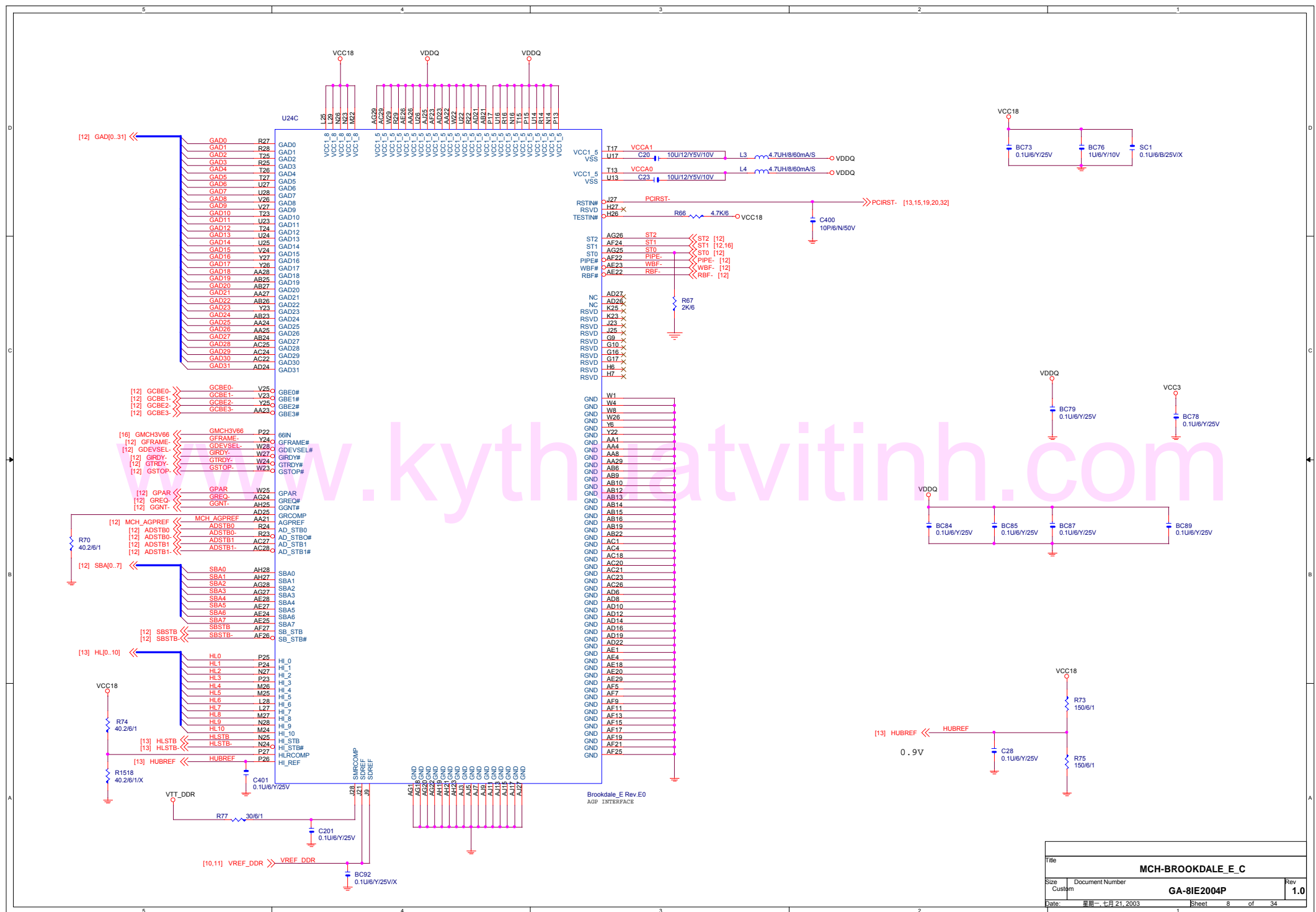
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		VCC SIDE (1 oz. Copper)	
		GND SIDE (1 oz. Copper)	
		SOLDER SIDE (0.5 oz. Copper)	
GIGABYTE			
Title COVER SHEET			
Size Custom	Document Number GA-8IE2004P		Rev 1.0
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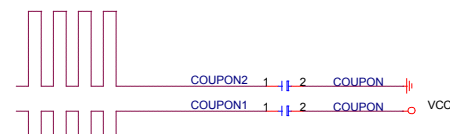
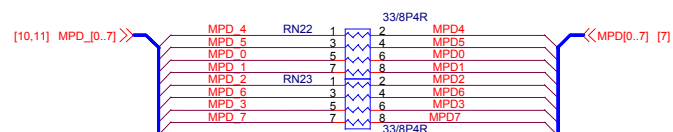
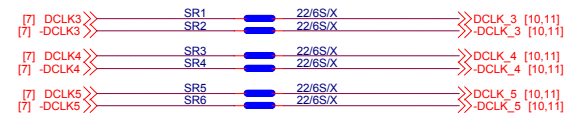
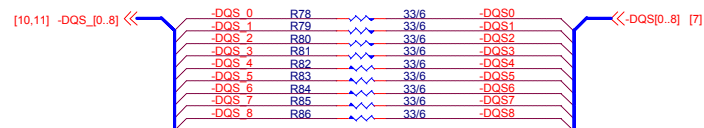
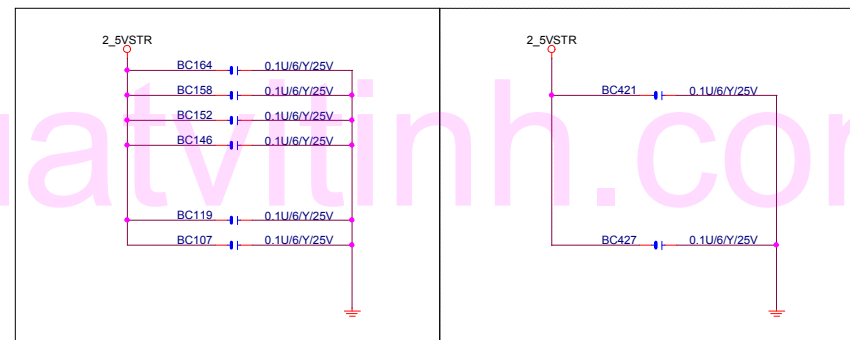
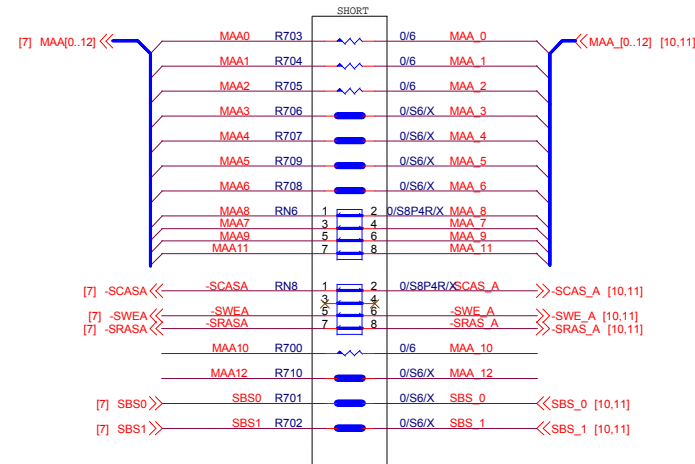


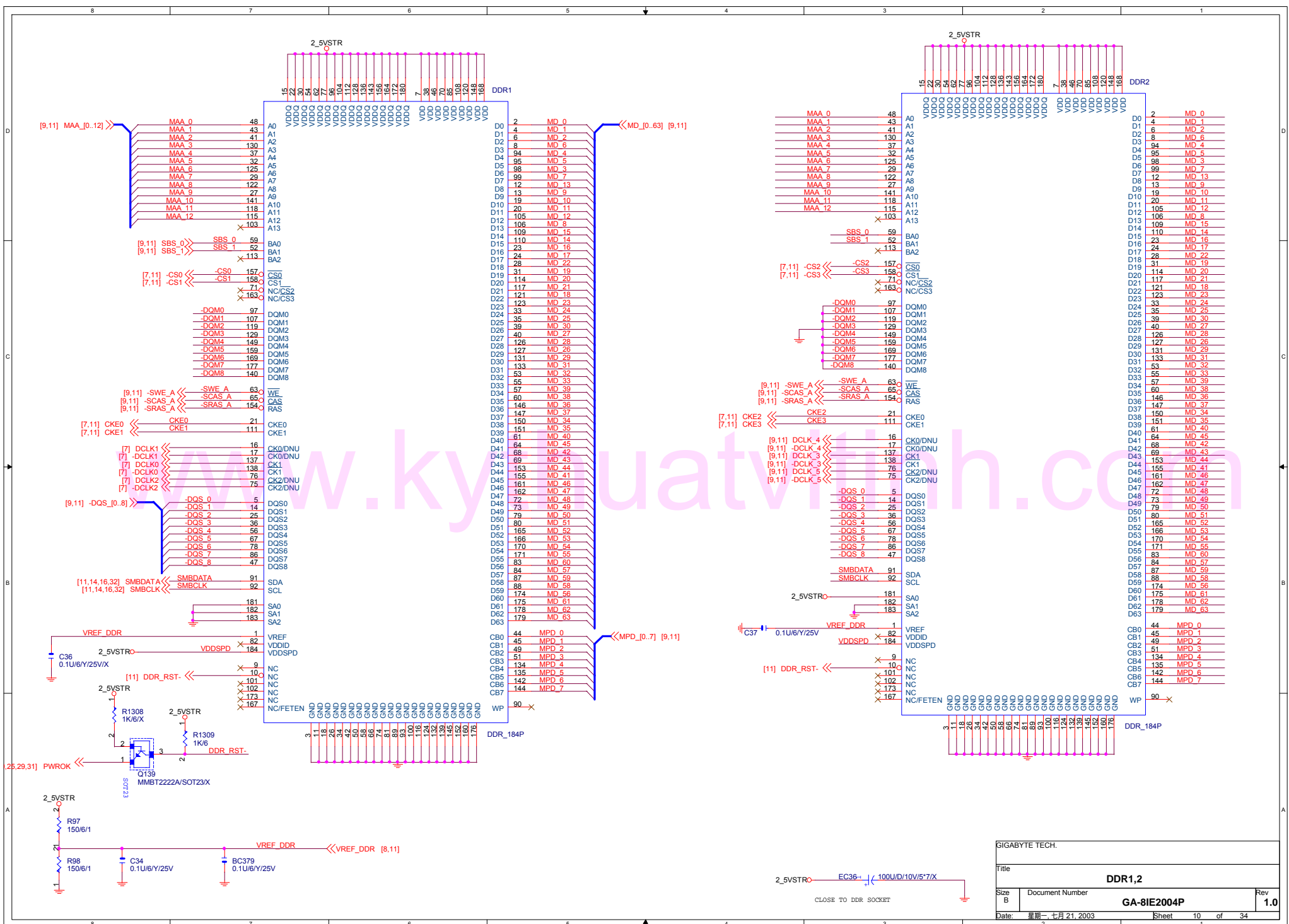


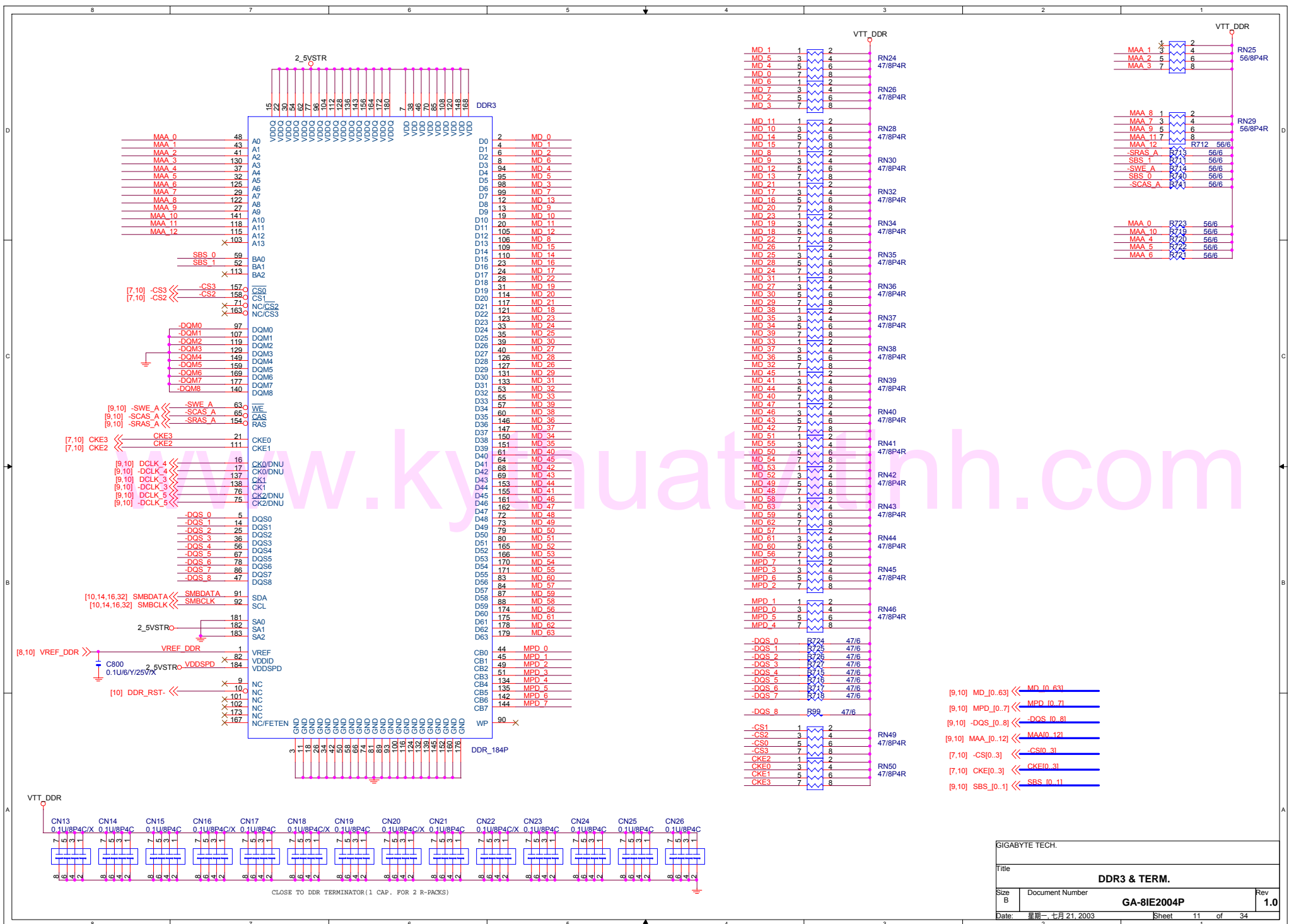


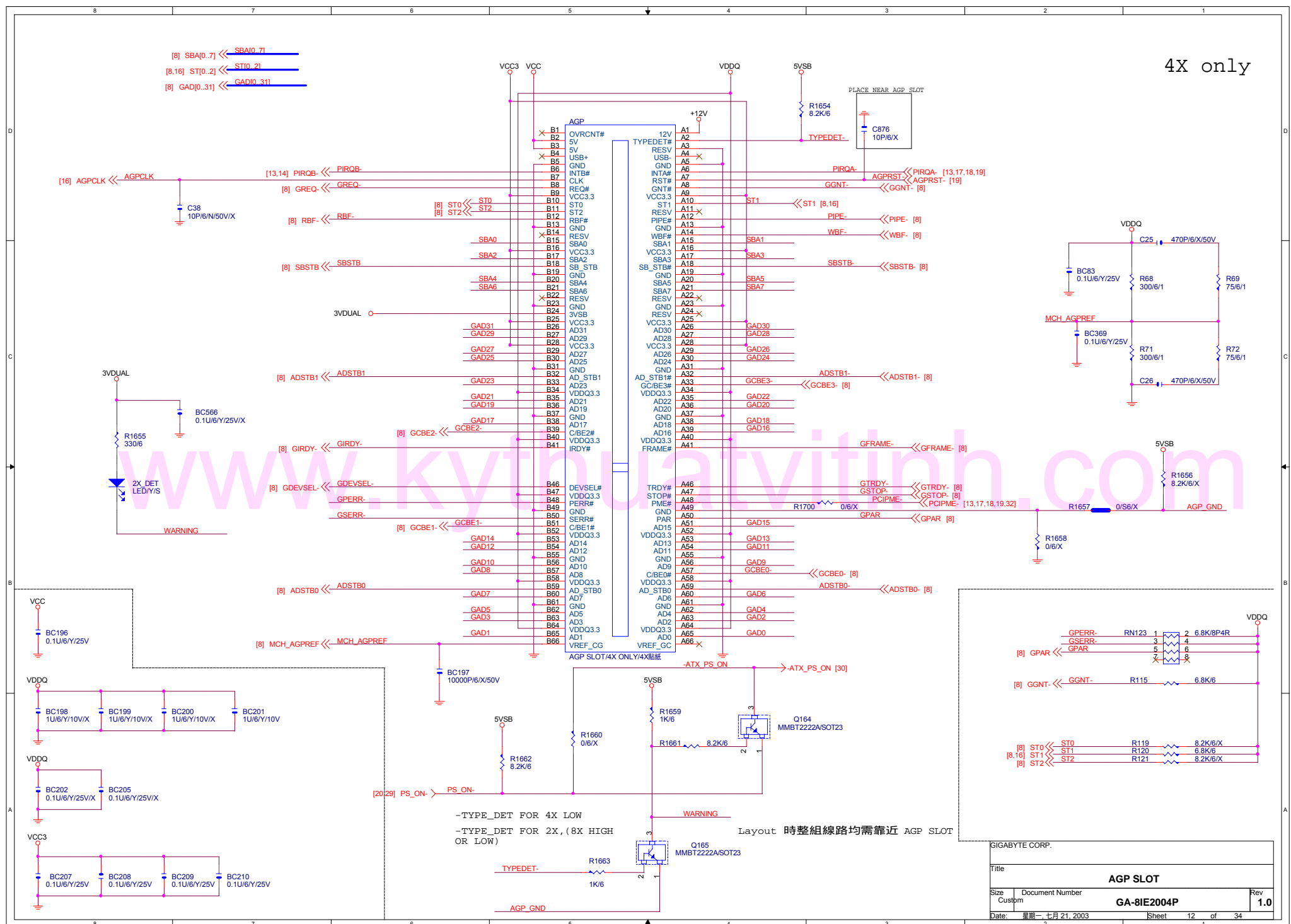


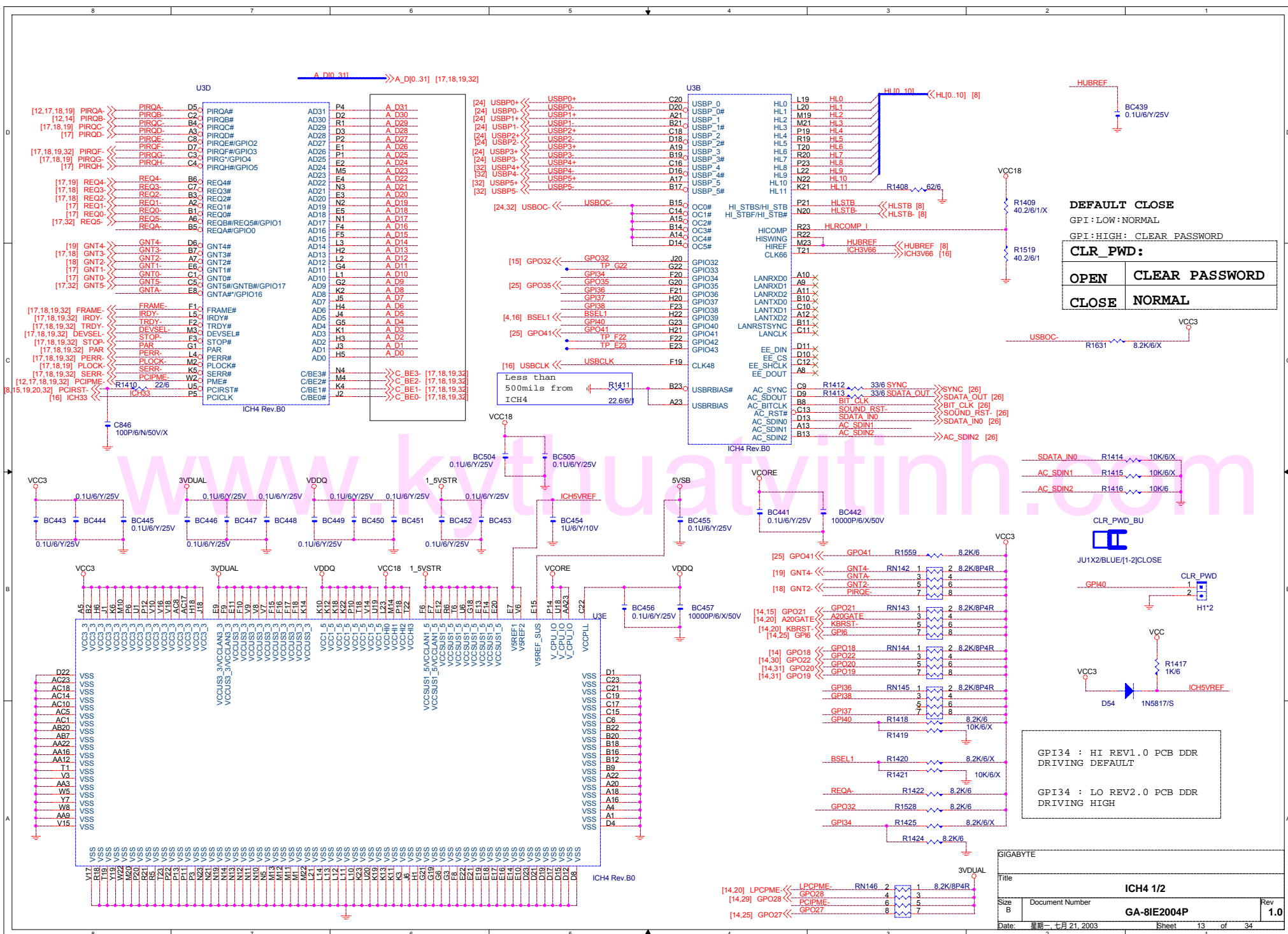


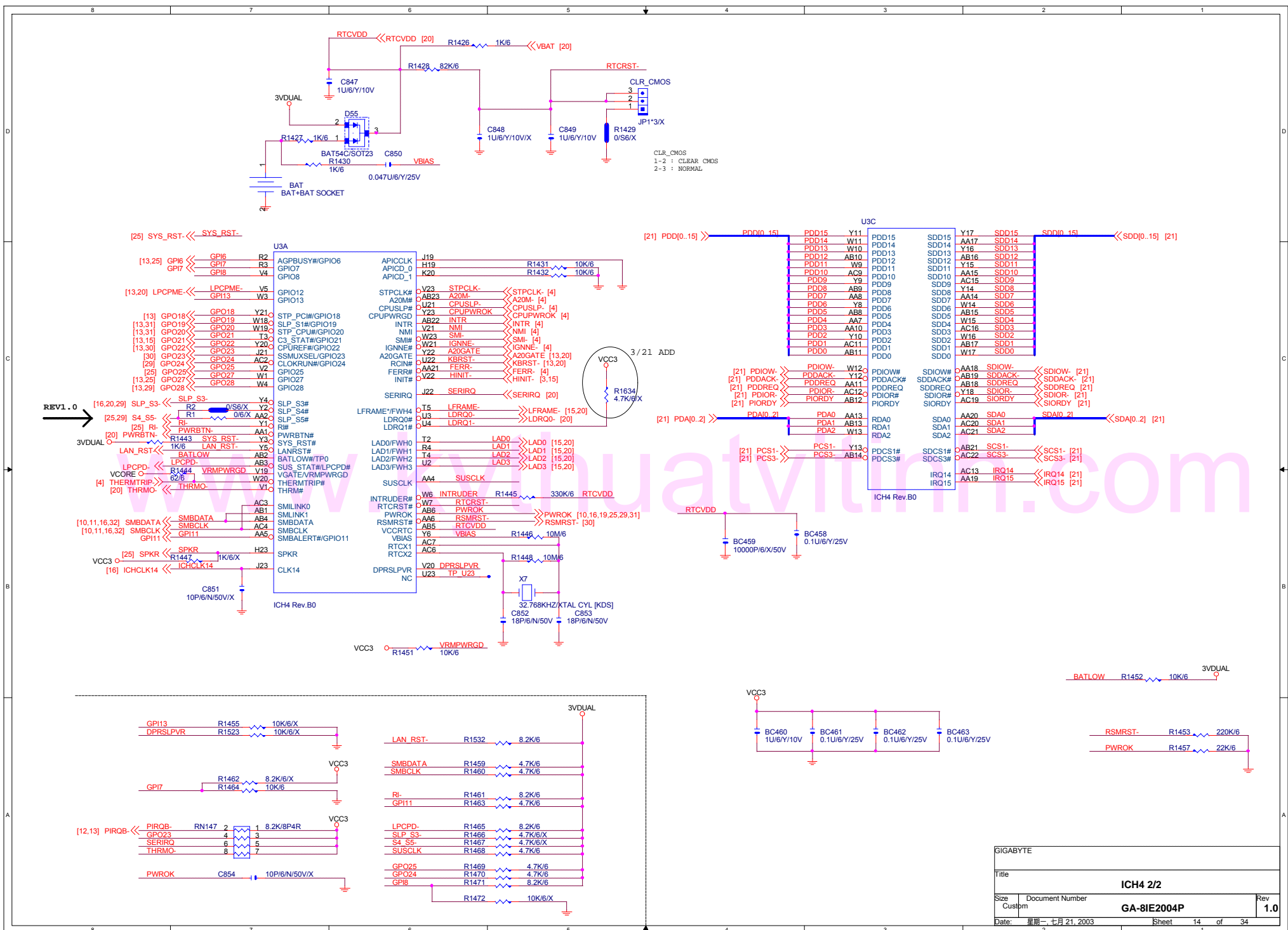




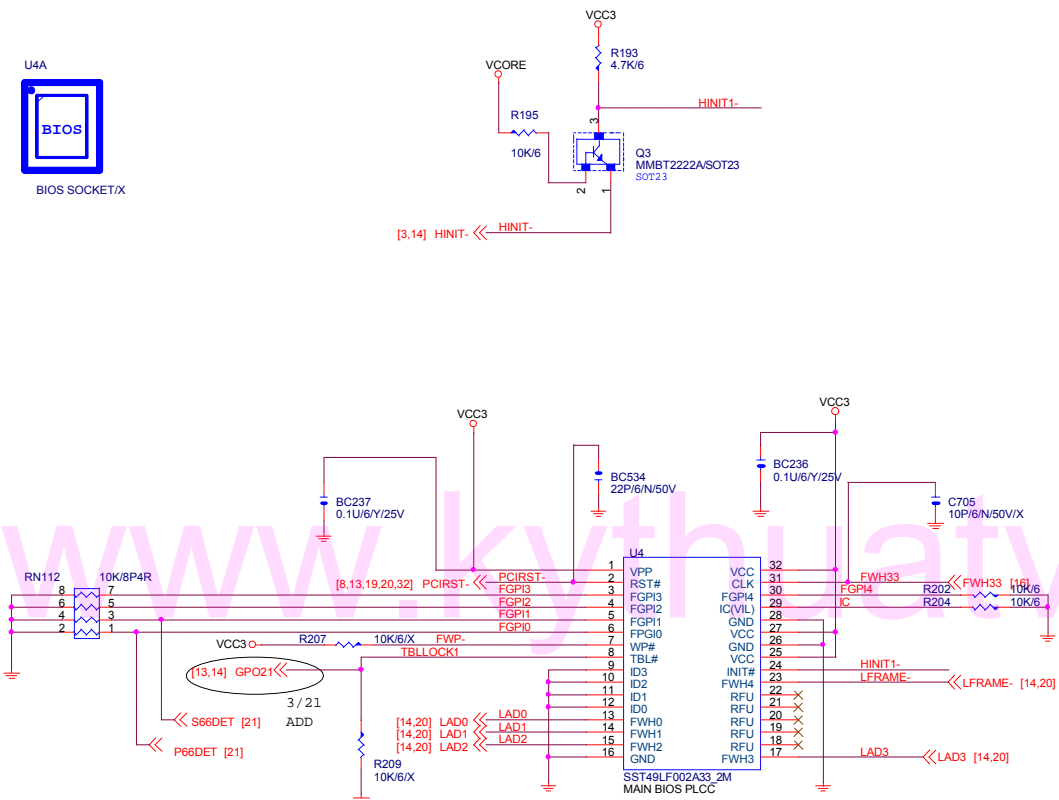
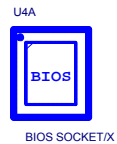


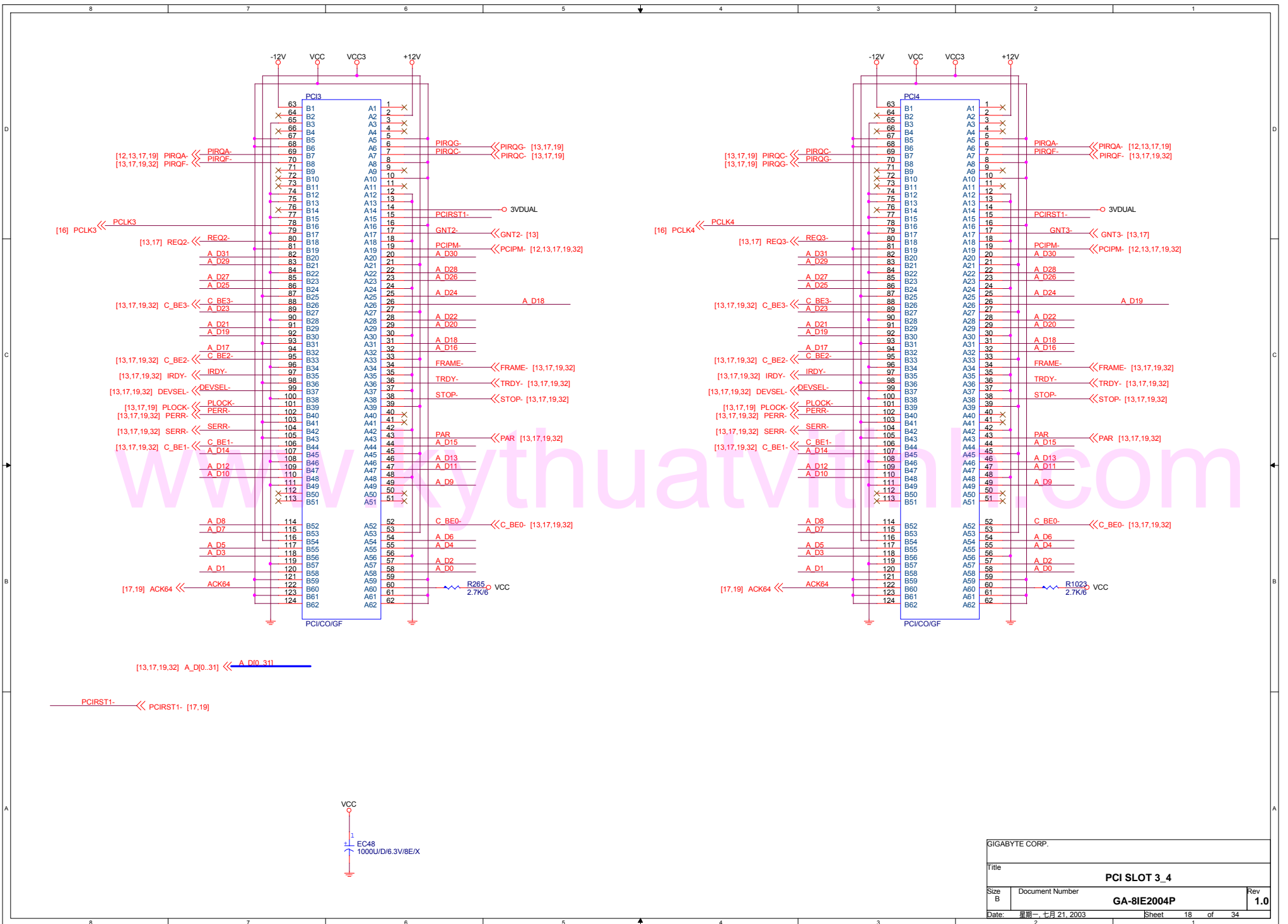


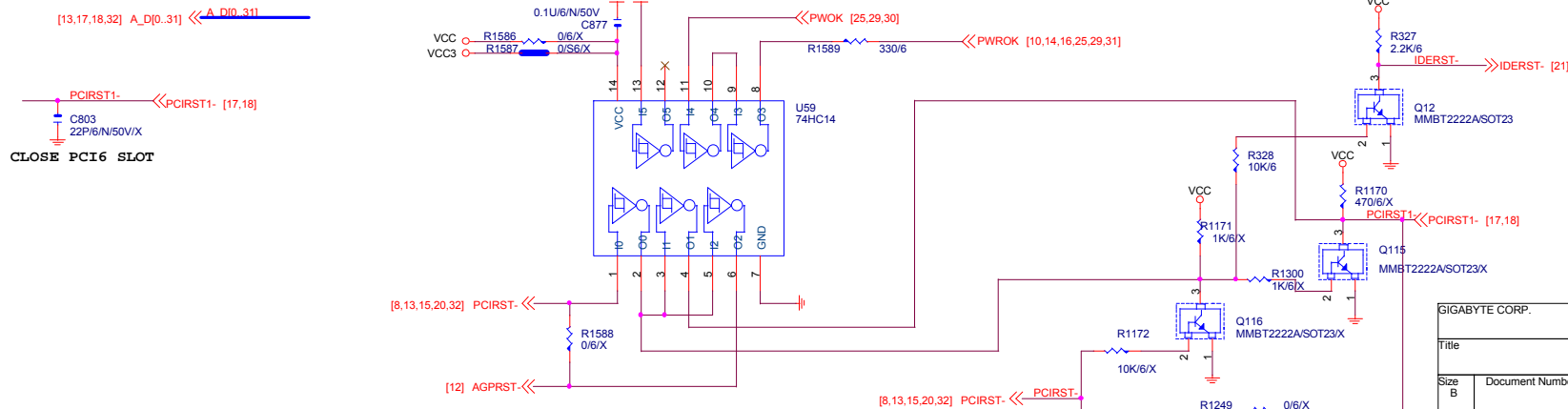
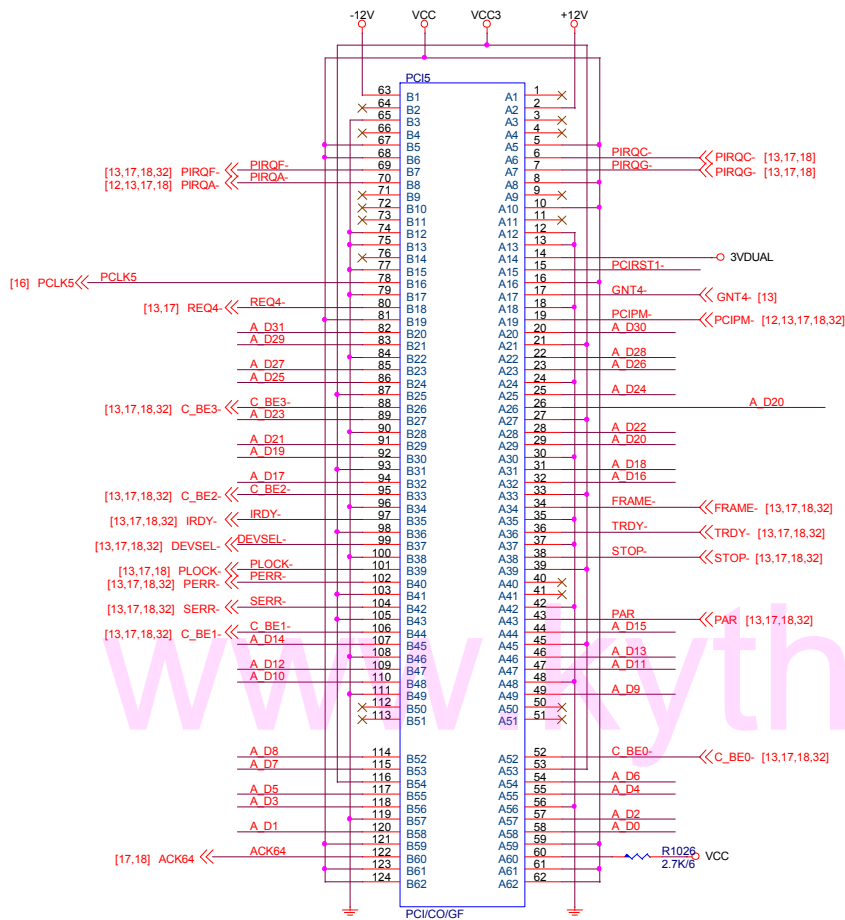




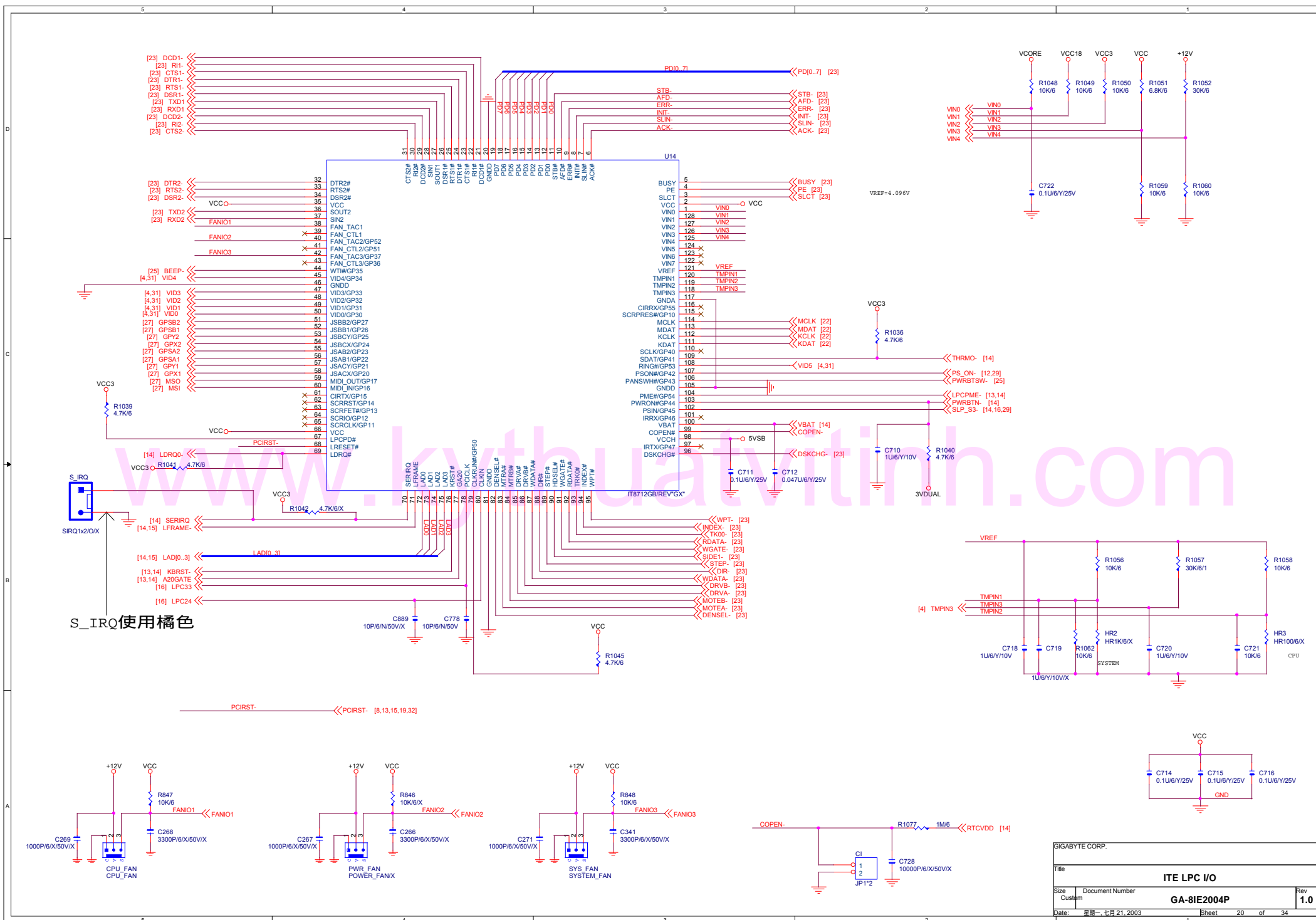
2002/04/15 MODIFY WRITE PROTECT

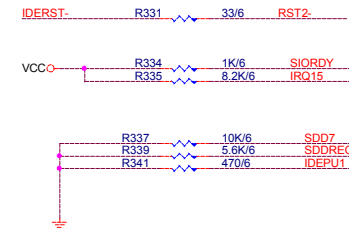
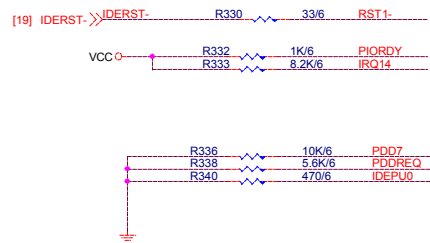
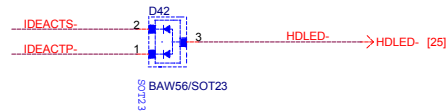






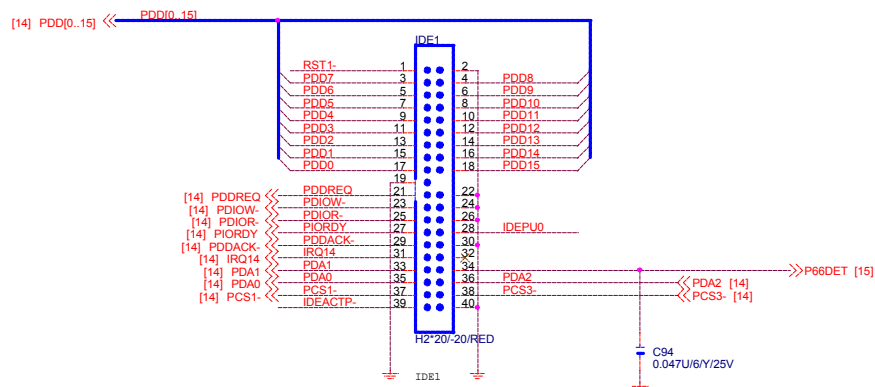
GIGABYTE CORP.		
Title		
PCI SLOT 5		
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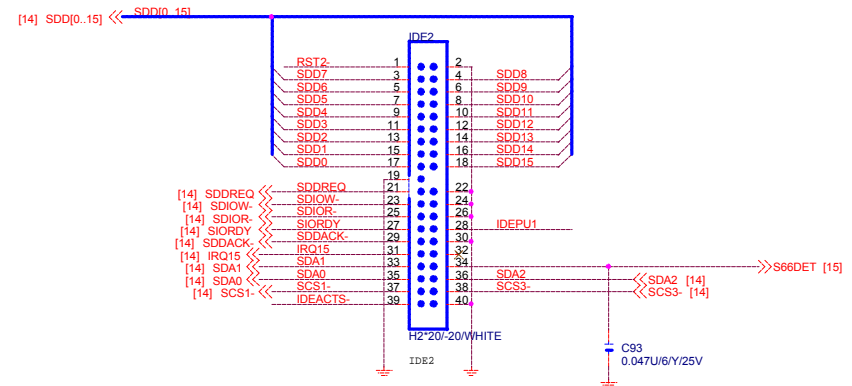
www.kythuatchitinh.com

PRIMARY IDE CONNECTOR



BIOS:CABLE DETECT AND DEVICE DETECT

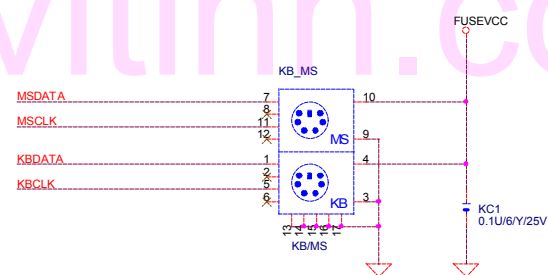
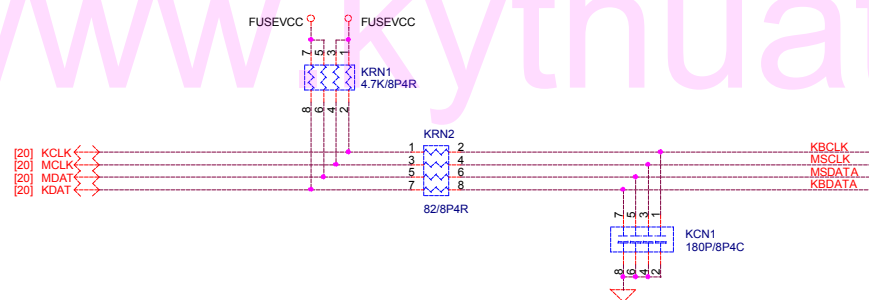
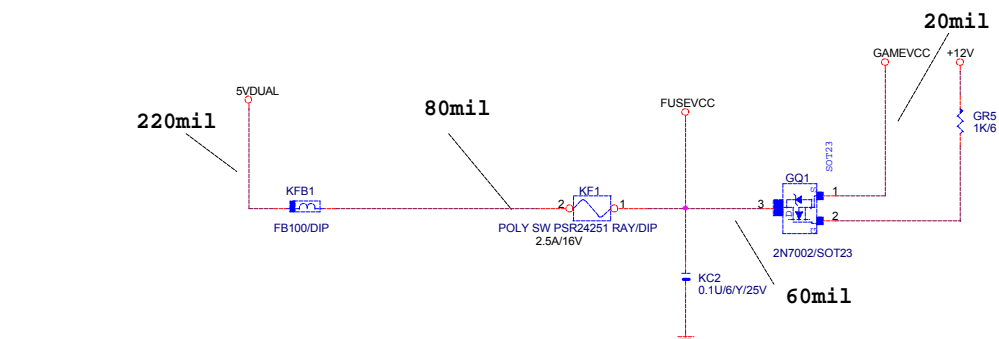
SECONDARY IDE CONNECTOR



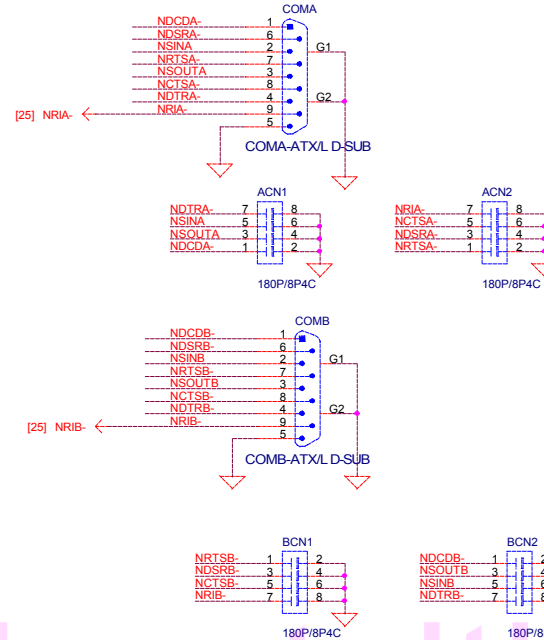
GIGABYTE CORP.

Title		
IDE CONNECTOR		
Size	Document Number	Rev
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Date	Sheet	of
2003 年 7 月 21 日	21	34

模組化線路



模組化線路



VCC

RN76
470/8P4R

R350
470/6

FDD

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34

FLOPPY

DENSEL- [20]

INDEX- [20]

MOTEA- [20]

DRVB- [20]

DRVA- [20]

MOTEB- [20]

DIR- [20]

STEP- [20]

WDATA- [20]

WGATE- [20]

TK00- [20]

WPT- [20]

RDATA- [20]

SIDE1- [20]

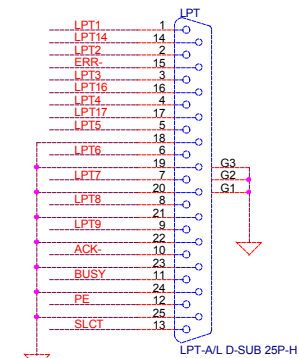
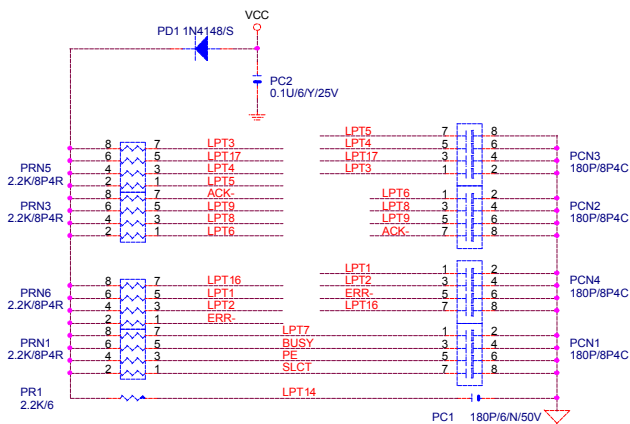
DSKCHG- [20]

The diagram shows the pin connections for the BU1 chip. The pins are numbered 1 through 20. The connections are as follows:

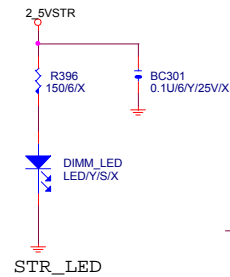
- Pins 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1 are connected to various components.
- Pins 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1 are connected to various components.
- Pins 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1 are connected to various components.

The diagram illustrates the 33/8P4R interface connections for three PRN (Peripheral Resource Number) blocks: PRN7, PRN4, and PRN2. Each PRN block is represented by a blue square with a wavy pattern, indicating a 33/8P4R interface. The connections are as follows:

- PRN7:**
 - Input [20] AFD- connects to AFD- (pin 1).
 - Input [20] STB- connects to STB- (pin 3).
 - Input [20] PD0 connects to PD0 (pin 5).
 - Input [20] INIT- connects to INIT- (pin 7).
 - Output LPT14 (pin 2) connects to LPT1.
 - Output LPT1 (pin 4) connects to LPT2.
 - Output LPT2 (pin 6) connects to LPT16.
- PRN4:**
 - Input [20] SLIN- connects to SLIN- (pin 1).
 - Input [20] PD2 connects to PD2 (pin 3).
 - Input [20] PD3 connects to PD3 (pin 5).
 - Output LPT3 (pin 2) connects to LPT17.
 - Output LPT4 (pin 4) connects to LPT4.
 - Output LPT5 (pin 6) connects to LPT5.
- PRN2:**
 - Input [20] ERR- connects to ERR- (pin 1).
 - Input [20] ACK- connects to ACK- (pin 3).
 - Input [20] BUSY- connects to BUSY- (pin 5).
 - Input [20] PE connects to PE (pin 7).
 - Output LPT6 (pin 2) connects to LPT8.
 - Output LPT8 (pin 4) connects to LPT9.
 - Output LPT9 (pin 6) connects to LPT7.







Filter Cap design:

FOR 650 DESIGN DEFAULT 由
CLOCK GEN來

FOR 650 DESIGN DEFAULT
不上CRYSTAL



Title

AC97

Size

Document Number

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Rev

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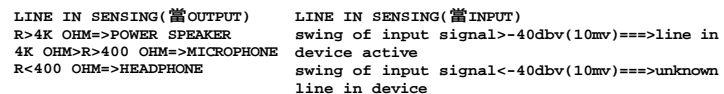
Date _____

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4	
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模組化線路

[illegible]

AUX_IN

[26] AUX_L ←

[26] AUX_R ←

1000P/6 FOR EMI

C6 1000P/6/X/50V/X

C7 1000P/6/X/50V/X

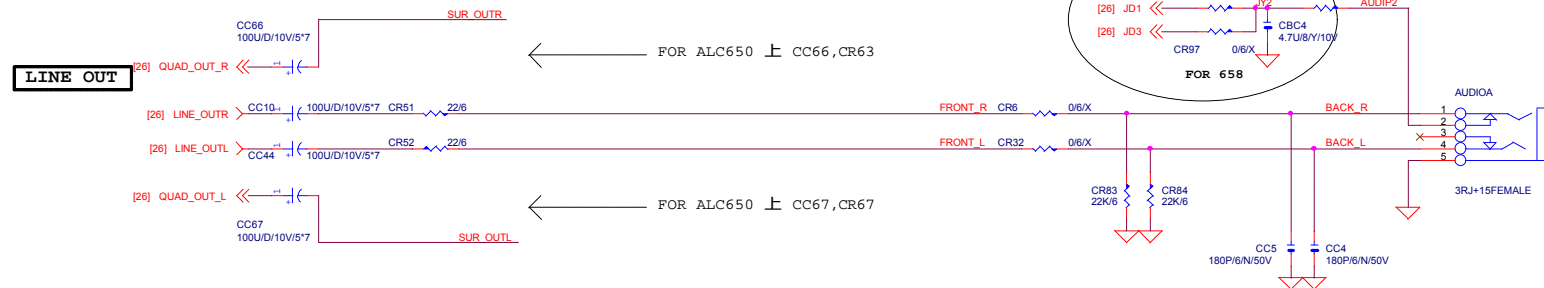
1 2 3 4

AUX_IN*4 HEADER[W]

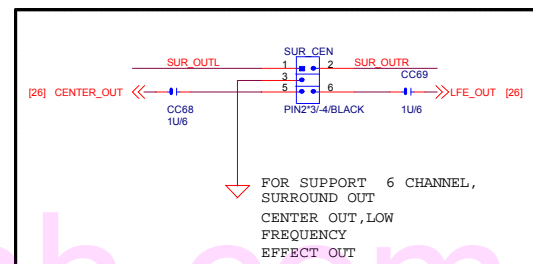
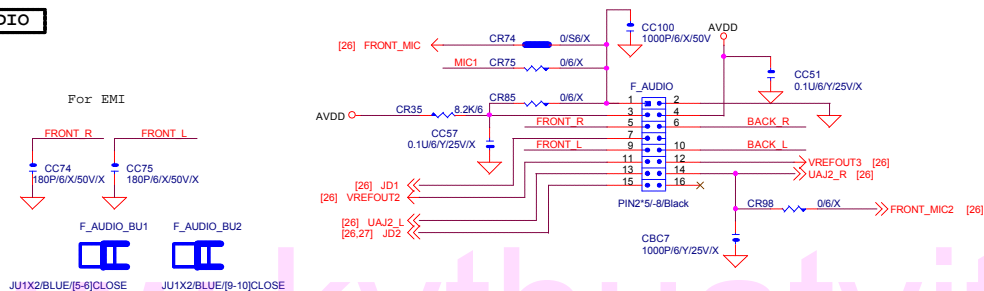
模組化線路

JDO,JD2,GPIO0 為偵測DEVICE INPUT 時由LOW
TO HIGH Edge trigger(pop manual)

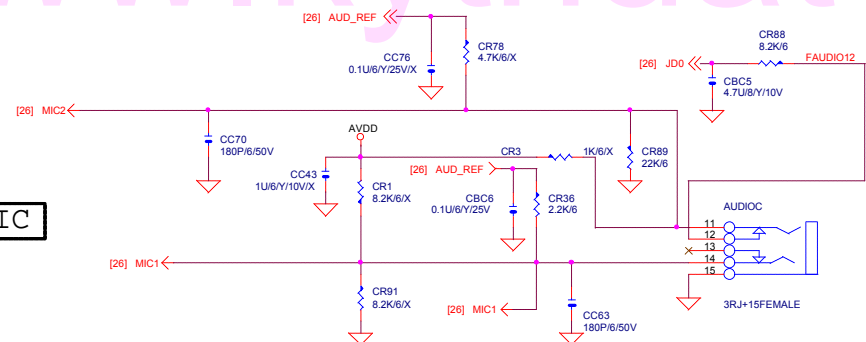
1/2(3.14)RC=1/2(3.14)8.2K*4.7U=4.3HZ 以上AC 信號全部衰減 TO OV
不會造成JDO 誤動作(無device 時play wav)



INTEL FRONT AUDIO



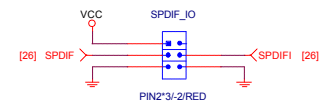
MIC



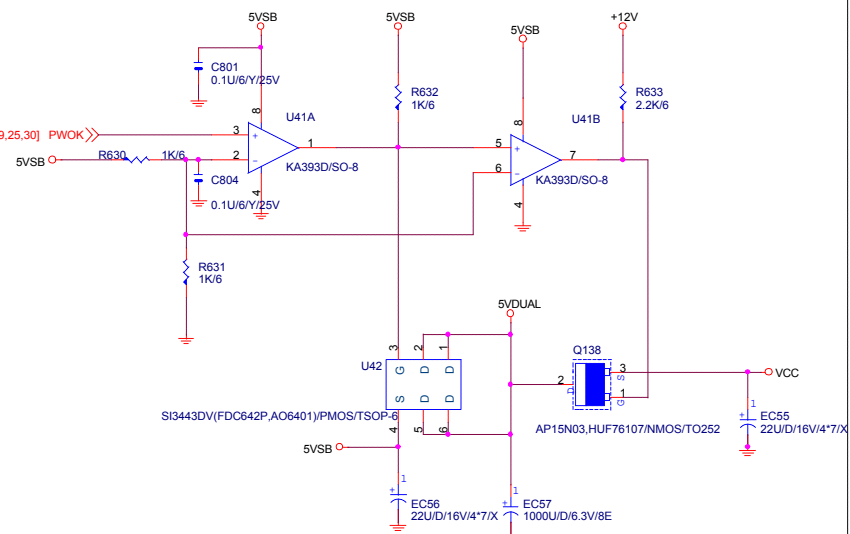
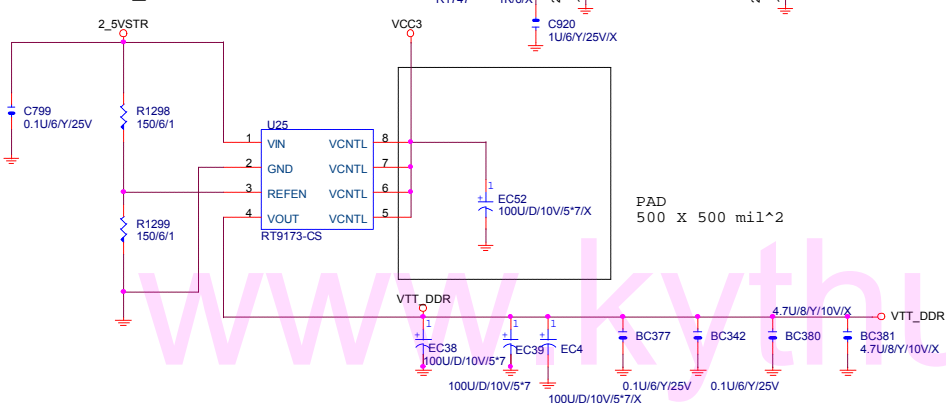
MICROPHONE IN SENSING(當INPUT)(利用vref 偏壓
與CR43,CR32 並聯求出阻抗)
7.1k ohm>R>2.3k ohm==>microphone in
R<2.3k ohm or R>7.1k ohm==>unknown device

MICROPHONE IN SENSING(當OUTPUT)
R>4K OHM=>POWER SPEAKER
4K OHM>R>400 OHM=>MICROPHONE
R<400 OHM=>HEADPHONE

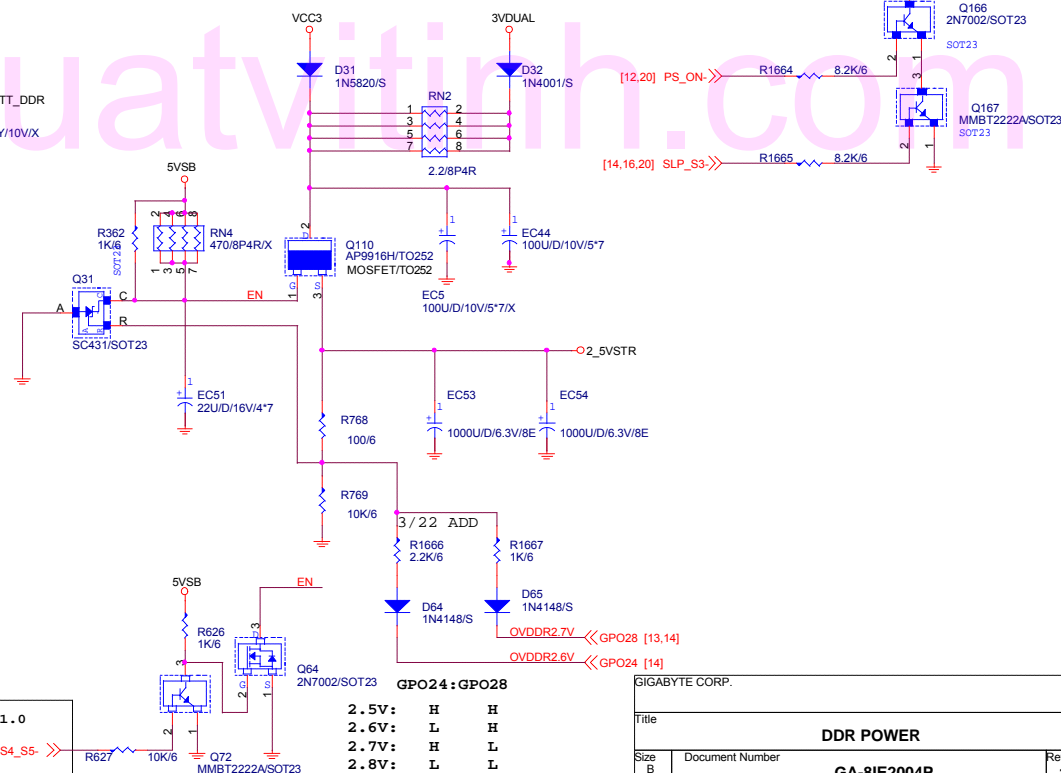
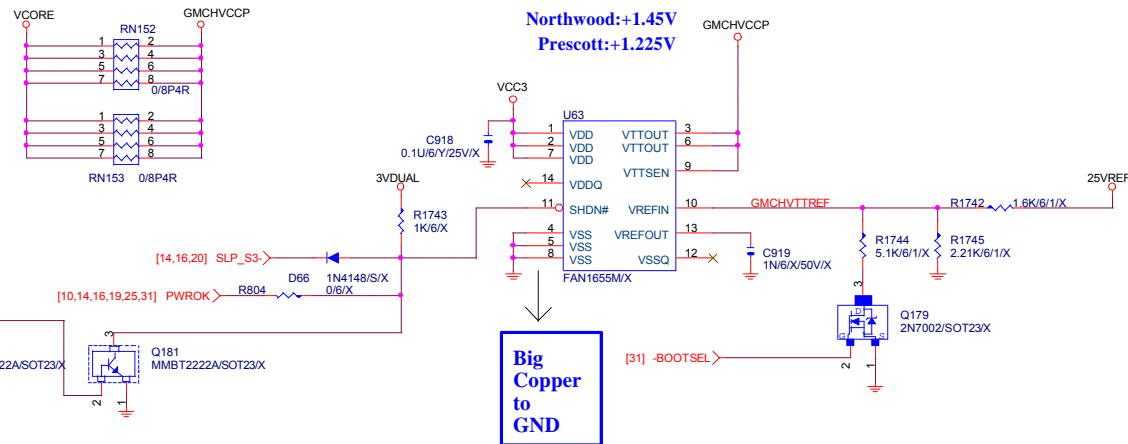
SPDIF_IO



1.25V VTT_DDR LINEAR SOLUTION



5VDUAL CIRCUIT



REV1.0

[14,25] S4_S5- >>

GPO24: GPO28

2.5V:	H	H
2.6V:	L	H
2.7V:	H	L
2.8V:	L	L

GIGABYTE CORP.

Title			DDR POWER
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CPU Voltage ID output

VCC3

RN1511 2 1K/8P4R VID3

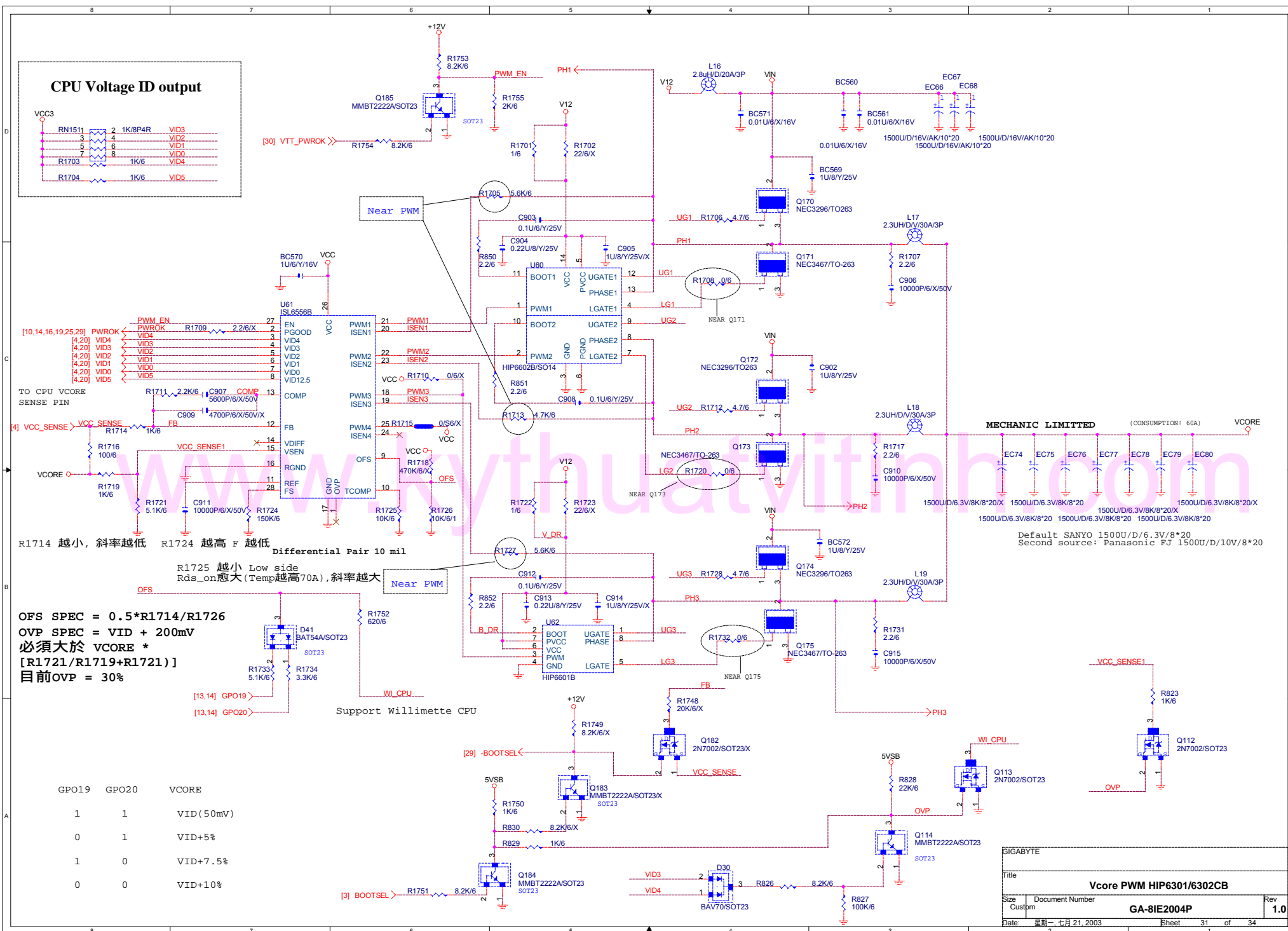
3 4 VID2

5 6 VID1

7 8 VID0

R1703 1K/6 VID4

R1704 1K/6 VID5



GIGABYTE			
Title			
Vcore PWM HIP6301/6302CB			
Size	Document Number	Re	
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LU1:
100M:RTL8100C

LR15:
100M:5.9K/6/1

LR4:
93C46:N/A
93C56:8.2K/6

DVD

LQ3:
100M:2N2907A
1G:N/A

Close to USB

When Inetl & GBT Gigabit (8110S)
Note: LEDS1-0 must set to 00 in EEPROM

GIGABYTE

LAN RTL8100CGA-8IE2004PRev
1.0

GIGABYTE GA-8IE2004P GPIO LIST

Revision 1.0

SHEET

TITLE

GPI		
GPI0/REQA-	NA	PULL 8.2K TO VCC3
GPI1/REQ5-		PULL 2.7K TO VCC
GPI2/PIRQE-	ID	PULL 8.2K TO VCC3 (default)
GPI3/PIRQF-		PULL 8.2K TO VCC3
GPI4/PIRQG-		PULL 8.2K TO VCC3
GPI5/PIRQH-	ID	PULL 8.2K TO VCC3 (default)
GPI6		PULL 8.2K TO VCC3 (GREEN BUTTON)
GPI7		PULL DOWN 10K TO GND
GPI8	ID	PULL 8.2K TO VCC3 (default)
GPI9	NA	NOT IMPLEMENTED
GPI10	NA	NOT IMPLEMENTED
GPI11		PULL 4.7K TO 3VDUAL (SMBALERT)
GPI12/LPCPME-		PULL 8.2K TO 3VDUAL (PME-)
GPI13		NC
GPI14	NA	NOT IMPLEMENTED
GPI15	NA	NOT IMPLEMENTED

SHEET

TITLE

GPO		
GPO16	NA	PULL 8.2K TO VCC3 (CAN'T PULL DOWN)因為會decode bios address 不正確:FF
GPO17		PULL 8.2K TO VCC3 (GNT5-)
GPO18	NA	PULL 8.2K TO VCC3 此OUTPUT 會TOGGLE.(在開機時).BIOS POST OK
GPO19		PULL 8.2K TO VCC3
GPO20		PULL 8.2K TO VCC3
GPO21		PULL 8.2K TO VCC3 (TOP BLOCK)
GPO22		PULL 8.2K TO VCC3
GPO23		PULL 8.2K TO VCC3
GPO24		PULL 4.7K TO 3VDUAL
GPO25		PULL 4.7K TO 3VDUAL (POWER LED)
GPO26		NOT IMPLEMENTED
GPO27		PULL 8.2K TO 3VDUAL (POWER LED)
GPO28		PULL 8.2K TO 3VDUAL
GPO32		PULL 8.2K TO 3VDUAL (BIOS WRITE PROTECT)
GPO35		PULL DOWN 10K TO GND (POWER LED)

COMPONENT SIDE (0.5 oz. Copper)	
VCC SIDE (1 oz. Copper)	
GND SIDE (1 oz. Copper)	
SOLDER SIDE (0.5 oz. Copper)	
GIGABYTE	
Title GPIO LIST	
Size Custom	Document Number GA-8IE2004P
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[illegible]

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<h1 style="margin: 0;">GIGABYTE</h1>		
Title		
<h2 style="margin: 0;">PCI ROUNT LIST</h2>		
Size Custom	Document Number	Rev
	<h3 style="margin: 0;">GA-8IE2004P</h3>	<h3 style="margin: 0;">1.0</h3>
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